In the Claims:

Kindly delete claims 1-27.

Please add the following claims:

28. An electrode, comprising:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said insulative layer, wherein said first portion and said second portion are different materials.

29. The electrode as specified in Claim 28, wherein said second portion and said third portion are different materials.

30. The electrode as specified in Claim 29, wherein said first portion and said third portion are different materials.

31. An dynamic random access memory device, comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said

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Sub B3 Concld.

insulative layer, wherein said first portion and said second portion are different materials.

32. The electrode as specified in Claim 31, wherein said second portion and said third portion are different materials.

33. The electrode as specified in Claim 32, wherein said first portion and said third portion are different materials.

Sub B4

34. An dynamic random access memory device, comprising:

a capacitor which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and at least a portion of said insulative layer, wherein said first portion and said second portion are different materials.

35. The electrode as specified in Claim 34, wherein said second portion and said third portion are different materials.

36. The electrode as specified in Claim 35, wherein said first portion and said third portion are different materials.

37. The dynamic random access memory device as specified in Claim 34, further comprising a transistor.

38. The dynamic random access memory device as specified in Claim 34, further comprising:

a) a dielectric layer overlying said third portion; and

b) a cell plate electrode overlying said dielectric layer.

39. An electrode, comprising:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are different materials.

40. The electrode as specified in Claim 39, wherein said second portion and said third portion are different materials.

41. The electrode as specified in Claim 40, wherein said first portion and said third portion are different materials.

42. The electrode as specified in Claim 39, further comprising a fourth portion

a6 cont'd.

interposed between said first and said second portions.

43. The electrode as specified in Claim 42, wherein the fourth portion reduces contact resistance between said first and said second portions.

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44. The electrode as specified in Claim 39, wherein said first portion is a silicon contact.

45. The electrode as specified in Claim 39, wherein said second portion is a diffusion barrier layer prohibiting diffusion of atoms between said first and said second portions.

46. The electrode as specified in Claim 39, wherein said third portion is an oxidation resistant layer.

47. The electrode as specified in Claim 39, wherein said insulative layer surrounds a lower sidewall of said third portion.

sub A6

48. A dynamic random access memory device, comprising:

an electrode which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are

different materials.

49. The electrode as specified in Claim 48, wherein said second portion and said third portion are different materials.

50. The electrode as specified in Claim 49, wherein said first portion and said third portion are different materials.

51. A dynamic random access memory device, comprising:

a capacitor which comprises:

a) a first portion formed in an insulative layer;

b) a second portion overlying the first portion, wherein said insulative layer surrounds a sidewall of said second portion; and

c) a third portion overlying said second portion and extending above an upper surface of said insulative layer, wherein said first portion and said second portion are different materials.

52. The electrode as specified in Claim 51, wherein said second portion and said third portion are different materials.

53. The electrode as specified in Claim 52, wherein said first portion and said third portion are different materials.

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54. The dynamic random access memory device as specified in Claim 51, further comprising:

Sub J1

a) a dielectric layer overlying said third portion; and

b) a cell plate electrode overlying said dielectric layer.

55. The dynamic random access memory device as specified in Claim 51 further comprising a transistor.

Sub B2

56. An electrode, comprising:

a) a contact formed in an insulative layer;

b) a diffusion barrier portion overlying said contact, said insulative layer surrounding a sidewall of said diffusion barrier portion; and

c) an oxidation resistant portion overlying said diffusion barrier portion and extending above an upper surface of said insulative layer, said diffusion barrier portion configured to inhibit diffusion of atoms between said contact and said oxidation resistant portion.

Sub J1

57. The electrode as specified in Claim 56, further comprising a reducing contact resistance portion interposed between said contact and said diffusion barrier portion, said reducing contact resistance portion configured to reduce a contact resistance between said contact and said diffusion barrier portion.

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58. A method for fabricating an electrode, comprising the following steps:

a) forming an insulative layer;

b) forming an opening in the insulative layer;

c) forming a first portion of the electrode in a lower region of the opening;

d) forming a second portion of the electrode in the opening and overlying the first portion, said insulative layer encompassing a sidewall of said second portion; and

e) forming a third portion of the electrode overlying the second portion and overlying at least a portion of the insulative layer, wherein said first portion and said second portion are different materials.

59. The electrode as specified in Claim 58, wherein said second portion and said third portion are different materials.

60. The electrode as specified in Claim 59, wherein said first portion and said third portion are different materials.

61. A method for fabricating an electrode, comprising the following steps:

a) forming an insulative layer;

b) forming an opening in the insulative layer;

c) forming a first portion of the electrode in a lower region of the opening;

d) forming a second portion of the electrode in the opening and overlying the first

portion, said insulative layer encompassing a sidewall of said second portion; and

e) forming a third portion of the electrode overlying the second portion and extending above a top surface of the insulative layer, wherein said first portion and said second portion are different materials.

62. The electrode as specified in Claim 61, wherein said second portion and said third portion are different materials.

63. The electrode as specified in Claim 62, wherein said first portion and said third portion are different materials.

64. The method as specified in Claim 61, further comprising the step of encompassing a lower sidewall of the third portion with said insulative layer.

65. The method as specified in Claim 61, further comprising the step of forming a fourth portion underlying the second portion and overlying the first portion.

66. The method as specified in Claim 61, wherein said step of forming said insulative layer comprises the following steps:

a) depositing a first portion of said insulative layer to overlie said substrate; and

b) depositing a second portion of said insulative layer to overlie said first portion of said insulative layer, said second portion of said insulative layer having oxidation

A6 Cont'd.

resistant properties.

67. The method as specified in Claim 66, further comprising the following steps:

a) patterning said second portion of said insulative layer to define the opening; and

b) removing exposed regions of said first and second portions of said insulative layer to create the opening.

68. The method as specified in Claim 66, further comprising the step of planarizing said first portion of said insulative layer.

69. A method for fabricating an electrode, comprising the following steps:

a) forming a recess in an electrically insulative layer to expose a substrate;

b) forming a contact in the recess overlying and in electrical contact with the substrate;

c) forming a diffusion barrier layer in the recess and overlying the contact;

d) forming a conductive oxidation resistant layer in the recess and overlying the diffusion barrier layer;

e) removing portions of the conductive oxidation resistant layer lying outside of the recess; and

f) removing portions of the insulative layer to expose an upper sidewall of said conductive oxidation resistant layer, said diffusion barrier layer inhibiting diffusion of

R6 Cont'd

atoms between said contact and said conductive oxidation resistant layer.

70. The method as specified in Claim 69, further comprising the step of forming a reducing contact resistance layer interposed between said contact and said diffusion barrier layer, said reducing contact resistance layer configured to reduce a contact resistance between said contact and said diffusion barrier layer.

71. The method as specified in Claim 69, further comprising the following steps:

a) forming a further electrically insulative region in the recess to overlie the conductive oxidation resistant layer; and

b) removing the further electrically insulative region in the recess during said step of removing portions of the insulative layer to expose the conductive oxidation resistant layer in the recess.

72. The method as specified in Claim 69, wherein said step of removing portions of the conductive oxidation resistant layer comprises planarizing the conductive oxidation resistant layer.

73. The method as specified in Claim 69, further comprising the following steps:

a) forming a dielectric layer overlying the conductive oxidation resistant layer; and

b) forming a cell plate layer overlying the dielectric layer.

74. A method for fabricating a capacitor, comprising the following steps:

A6 Cont'd.

a) forming an electrically insulative layer overlying a substrate;

b) forming an opening in said insulative layer in order to expose said substrate;

c) forming a conductive plug in said opening, said conductive plug forming a first portion of a first electrode of said capacitor;

d) providing a recess in said opening between a surface of said insulative layer and a surface of said conductive plug;

e) forming a diffusion barrier layer in said recess such that a sidewall of said diffusion barrier layer is surrounded by said insulative layer, said diffusion barrier layer overlying said conductive plug and forming a second portion of said first electrode;

f) forming a conductive oxidation resistant layer overlying said insulative layer and in the recess overlying said diffusion barrier layer, said diffusion barrier layer configured to inhibit diffusion of atoms between said conductive plug and said conductive oxidation resistant layer;

g) removing portions of the conductive oxidation resistant layer overlying said insulative layer while retaining portions of said conductive oxidation resistant layer in the recess, remaining portions of the conductive oxidation resistant layer forming a third portion of said first electrode;

h) removing portions of said insulative layer to expose an upper portion of a sidewall of said conductive oxidation resistant layer;

i) retaining a portion of said insulative layer at a lower portion of said sidewall of

AC Cont'd.

said conductive oxidation resistant layer;

j) forming a dielectric layer overlying said conductive oxidation resistant layer; and

k) forming a second electrode overlying said dielectric layer, said first and said second electrodes and said dielectric layer forming the capacitor.

75. The method as specified in Claim 74, wherein said step of forming said insulative layer comprises the following steps:

a) depositing a first portion of said insulative layer to overlie said substrate; and

b) depositing a second portion of said insulative layer to overlie said first portion of said insulative layer, said second portion of said insulative layer having oxidation resistant properties.

76. The method as specified in Claim 75, further comprising the following steps:

a) patterning said second portion of said insulative layer to define the opening; and

b) removing exposed regions of said first and second portions of said insulative layer to create the opening.

77. The method as specified in Claim 76, further comprising the step of planarizing said first portion of said insulative layer.

a6 contd.

78. The method as specified in Claim 74, further comprising the steps of:

a) depositing a further insulative layer in said recess to overlie at least a portion of said conductive oxidation resistant layer; and

b) removing said further insulative layer during said step of removing portions of said insulative layer.

79. The method as specified in Claim 74, further comprising the step of forming a reducing contact resistance layer interposed between said conductive plug and said diffusion barrier layer, said reducing contact resistance layer configured to reduce a contact resistance between said contact and said diffusion barrier layer.

sub B9

80. A method for fabricating an electrode, comprising the following steps:

a) forming an electrically insulative layer overlying a substrate;

b) masking the insulative layer to define a future opening in the insulative layer;

c) etching the insulative layer in an exposed region to form the opening and to expose the substrate;

d) forming a contact to the substrate in the opening;

e) recessing a top surface of the contact from a surface of the insulative layer;

f) forming a diffusion barrier layer overlying the contact;

g) removing portions of the diffusion barrier layer overlying the insulative

Claim Cont'd.

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layer;

h) forming a conductive oxidation resistant layer overlying the diffusion barrier layer;

i) removing portions of the conductive oxidation resistant layer overlying the insulative layer; and

j) removing upper portions of the insulative layer to expose an upper sidewall of the conductive oxidation resistant layer, wherein said conductive oxidation resistant layer, said diffusion barrier layer, and said contact form the electrode.

81. The method as specified in Claim 80, wherein said step of forming an electrically insulative layer comprises the following steps:

a) depositing a first portion of said insulative layer to overlie said substrate; and

b) depositing a second portion of said insulative layer to overlie said first portion of said insulative layer, said second portion of said insulative layer having oxidation resistant properties.

82. The method as specified in Claim 80, further comprising the following steps:

a) creating a dielectric layer overlying the conductive oxidation resistant layer; and

b) creating a further electrode overlying the dielectric layer.

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83. The method as specified in claim 80, further comprising forming a reducing contact resistance region interposed between the contact and the diffusion barrier layer, said reducing contact resistance region configured to reduce a contact resistance between said contact and the diffusion barrier layer.

sub B10 >

84. A method for fabricating an electrode, comprising the following steps:

a) forming a contact overlying and in electrical contact with a substrate;

b) interposing a diffusion barrier layer between the contact and a conductive oxidation resistant layer, at least said diffusion barrier layer and said conductive oxidation resistant layer forming an electrode of said capacitor;

c) encompassing a sidewall of said diffusion barrier layer with an insulative layer, said insulative layer prohibited from overlying and underlying said diffusion barrier layer; and

d) encompassing a bottom portion of a sidewall of said conductive oxidation resistant layer with the insulative layer, a top portion of the sidewall extending above the insulative layer.

85. The method as specified in Claim 84, further comprising the following steps:

a) forming a dielectric layer overlying said conductive oxidation resistant layer;

b) applying a temperature capable of oxidizing said diffusion barrier layer;

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Sub B10 Concl'd. >

c) preventing oxidation of said diffusion barrier layer during said step of applying; and

d) forming a further electrode overlying said dielectric layer.

86. The method as specified in Claim 85, further comprising:

a) forming a plurality of the capacitors; and

b) providing electrical communication between said further electrodes of said plurality.

Sub B11 >

87. The method as specified in Claim 84, further comprising the following steps:

a) depositing said insulative layer to overlie said substrate prior to said step of forming the contact;

b) patterning said insulative layer to define a future opening; and

c) removing a portion of said insulative layer to create the opening in said insulative layer in which to form the contact.

Sub. H5

88. The method as specified in Claim 84, further comprising forming a reducing contact resistance region interposed between the contact and the diffusion barrier layer, said reducing contact resistance region configured to reduce a contact resistance between said contact and the diffusion barrier layer.---.

In the drawings:

Please insert additional figures 12-28, submitted herewith, into the patent application.

Respectfully submitted,

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SC/lab

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express mail in an envelope addressed to: Commissioner of Patents & Trademarks, Washington, D.C. 20231, on December 14, 1995.

____________________________ December 14, 1995.
Susan B. Collier, Agent of Record